Low-power design methodology and techniques – industrial perspective

SUMMARY

Power has become a critical metric and key differentiator in sub-65nm designs, due to growing power density driven by technology scaling and chip integration. This tutorial provides overview of the low-power design methodologies and techniques in production design perspective, emphasizing on the real design considerations and impact on chip success. We shall discuss pros and cons of the methods and techniques considering impacts on chip design schedule, yield, and overall power-performance target. We shall also provide design guidance and recommendations in various design steps and decision making points, based on our years of successful experience in production low-power SOC designs. This tutorial will start with overview of power related challenges in sub-60nm design and state-of-the-art power reduction techniques, and then detailed discussions about production low-power design methodology and techniques focusing on the power-gating and the voltage/frequency scaling which are the two advanced power reduction methods used effectively in sub-65nm production low-power designs. We shall explain when, where and how these methods and techniques should be applied to a chip based on the design goals and time-to-market requirement. We shall also cover production low-power design methodology and flow with power intent and unified design environment.

The objective of this half-day tutorial is to addresses the needs in low-power design industry.

PRESENTERS

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PRESENTERS BIOGRAPHIS

Kaijian Shi is Solution Architect in Cadence Design Systems, specializing in low-power design methodology and implementation. He has worked as a consultant on more than 11 leading-edge commercial low-power designs all taped out successfully. Dr. Shi is one of those in EDA and semiconductor industry who pioneer the low-power implementation methodology developments for production chip design. He has been a key contributor to the development of the advanced low-power production design flow in a leading semiconductor company which he has been consulting for. Dr. Shi co-authored the book "Low Power Methodology Manual for System-on-Chip Design" and has published 53 papers in journals and international conferences. He holds a Ph.D. degree from University of Kent at Canterbury, UK since 1994. Dr. Shi is Technical Program co-Chair of the 25th IEEE SoC Conference in 2012. He was Chairman of IEEE Dallas Section in 2006 and Chairman of IEEE Circuits and System Society Dallas Chapter in 2004. He was Workshop chair and then publicity chair of IEEE SoC Conference 2008-2011 and program committee members of IEEE ISVLSI (2006-2008) and DesignCon (2004-2008).

PRESENTERS' PUBLICATIONS (LOW-POWER RELATED)

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16. Kaijian Shi and Craig Godwin, "Hybrid Hierarchical Timing Closure Methodology for a High Performance and Low Power DSP", Proc. ACM/IEEE Design Automation Conference (**DAC**), June., 2003